# Noninvasive Leakage Power Tomography of Integrated Circuits by Compressive Sensing

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## ABSTRACT

We introduce a new methodology for *noninvasive post-silicon characterization of the unique static power profile (tomogram) of each manufactured chip*. The total chip leakage is measured for multiple input vectors in a linear optimization framework where the unknowns are the gate leakage variations. We propose *compressive sensing* for fast extraction of the unknowns since the leakage tomogram contains correlations and can be *sparsely represented*. A key advantage of our approach is that it provides leakage variation estimates even for inaccessible gates. Experiments show that the methodology enables fast and accurate noninvasive extraction of leakage power characteristics.

## Categories and Subject Descriptors

B.7.3 [**Integrated Circuits**]: Reliability and Testing; B.1.3 [**Hardware**]: Control Structure Reliability, Testing, and Fault-Tolerance; B.8.2 [**Performance and Reliability**]: Performance Analysis and Design Aids

## General Terms

Performance, Measurement, Verification

## Keywords

Post-silicon Characterization, Process Variations, Leakage Current

## 1. INTRODUCTION

The aggressive scaling of CMOS feature sizes is a result of the growing demand for lowering the cost-per-function by increasing the device density and computational speed. Because of the random inaccuracy in manufacturing at small scales, variations in transistor feature sizes are inevitable. As a result, VLSI circuits show highly variable power characteristics. The power consumption of an integrated circuit (IC) is not a deterministic function of the design anymore. Each chip exhibits a specific profile for both static and dynamic power consumptions.

This work is partly supported by the Defense Advanced Research Projects Agency (DARPA)/MTO Young Faculty Award (YFA), W911NF-07-1-0198, and by the National Science Foundation (NSF), 0716674.



*ISLPED'08,* August 11–13, 2008, Bangalore, India.



Post-silicon power characterization of an IC is a challenging and important task. Tomography is the general term used for imaging by sectioning. *Power tomography* refers to the task of finding the image of a chip's power variations in the 2D layout space. Characterizing a chip's power tomogram is the key enabler for a variety of applications, described in Section 3, such as power simulations and hot spot identification.

Modeling the statistical variations of device characteristics is a subject of active research [1–3]. In sub-100nm CMOS technology static power (leakage current) is a large portion of the total power consumption [4]. For example, cache leakage management leads to a 28% reduction in power consumption [5]. Estimation of the process variation for a manufactured IC is not easy. Although invasive methods have been proposed [2,6], the research in finding the specific power profile of each chip post-silicon has been limited. To date there is no general method for noninvasive estimation of the power variations across an IC.

In this paper, we use external leakage current measurements and the new theory of compressive sensing to find post-silicon tomogram of the static power profile of a manufactured chip. First, we apply a number of input vectors to the chip and measure the corresponding total leakage current. Next, we use the measurements and the combinational logic relations of the IC in a linear optimization framework. The unknown variables are the normalized leakage power consumption of each gate. The optimization objective is to decrease the discrepancy among the multiple measurements, while the constraints are provided by the measurements relations. Our key insight is that because of the spatial correlations in the gates' leakage currents, the gate leakage current vector can be sparsely represented [7, 8]. Thus, we propose compressed sensing to recover the sparse representation of the leakage variations in the wavelet domain using a small number of power measurements. Evaluation results show that by using the new method, the tomogram representing the IC's leakage power profile can be rapidly found with a low estimation error. Our contributions are as follows:

(1) We propose a new linear optimization framework for noninvasive extraction of the chip's leakage power profile.

(2) We report the first ever use of the novel theory of compressive sensing in characterizing the IC's variations.

(3) For the first time, the sparsity of the process variations is exploited for post-silicon characterization. Even though spatial correlations in process variations have been widely studied [2, 6, 9], using the sparsity resulting from the correlations for post-silicon power tomography is new.

(4) We accommodate the non-regular gate placements by modifying the original compressive sensing formulation.

(5) Using the method, we estimate leakage variations of the gates that are inaccessible because of uncontrollability and unobservability problems. The sparsity of the variations is the key for estimating the inaccessible gates.

(6) We show how the characterization result is insensitive to the choice of input vectors. This is because the compressive sensing theory is able to find a solution for random measurement inputs that are independent.

(7) We propose a number of new applications for noninvasive post-silicon tomography of the leakage power.

The remainder of the paper is as follows. Related work, applications and preliminaries are discussed in Section 2, 3 and 4, respectively. The framework for noninvasive chip tomography using leakage current measurements is presented in Section 5. The compressive sensing formulation of the problem is introduced in Section 6. Evaluation results are shown in Section 7. We summarize the paper in Section 8.

# 2. RELATED WORK

Although pre-silicon models of the statistical process variations are widely available [3, 10–12], there is a lack of research in post-silicon measurement and characterization. Doh et al. fabricated a $4 \times 5$ module array in 130nm CMOS technology to experimentally characterize spatial correlation in the process variation [6]. Friedberg et al. used Electrical Linewi- dth Metrology (ELM) to measure feature size of all transistors on a 200 mm wafer [2]. They used the Kelvin test to find linewidth by ELM measurements. They also proposed a piecewise linear model for spatial correlation function (correlogram). Zhao et al. used transistor arrays to study the process variation [9] of a test chip designed in [13]. The test structure was specifically designed to study local variation in the transistors. They proposed a method to model process variations and showed that knowing the statistical parameters of the variation can reduce the IC power prediction error from 30% to 7%. Hargreaves et al. [14] used separate measurements of ring oscillators' frequencies to measure variations of a test chip. The measured variations were modeled as a Gaussian field. Their method differs from the Gaussian model by Liu [10] in both the form of the correlation function and the fitting procedure.

All the above post-silicon variation studies are invasive. However, there is a need for noninvasive post-silicon characterization methods. We introduce a non-invasive post-silicon tomography that provides fast, inexpensive, and accurate estimate of each IC's unique variations.

# 3. APPLICATIONS

The fast chip tomography method reveals the specific leakage characteristics of each IC using only a small number of measurements. The method is inexpensive and enables investigation of a wide spectrum of important and challenging new post-silicon applications, including:

(1) *Leakage variation modeling and simulation.* Statistical modeling of chip variations has been an active area of research [1, 10, 12]. Instead of using typical parametric models such as the common assumption of multivariate normal distribution, researchers can use the post-silicon tomogram of the manufactured ICs to form nonparametric models that more accurately express the leakage variations. These models can also be integrated within power simulator tools for accurate and realistic simulation models.

(2) *Identifying the hot spots.* Finding the tomogram of the chip enables identification of those hot-spots that incur a larger leakage power dissipation. Hot spots can be specifically controlled or cooled down to avoid possible damages.

(3) *Post-silicon optimization.* Knowing the variations in an IC helps us to find the true power consumption of the different parts of the IC. Thus, one can perform efficient IC-specific power optimizations. For example, Alkabani et al. [15] recently showed that IC-specific post-silicon input vector control in average results in 10% more leakage power reduction compared with pre-silicon input control in the 90nm technology.

(4) *Fault detection.* When a digital IC is designed and manufactured, there is no guarantee that it has the same functionality as it is designed; i.e., there might be some faulty logic gates that affect the IC's functionality. Thus, the manufactured IC should be tested for faulty gates [16]. One can use the leakage power tomography results to detect the faulty gates that represent abnormal characteristics.

(5) *IC identification and fingerprinting.* The leakage power tomogram is specific to each chip and thus provides a unique signature (fingerprint) for the pertinent IC. It is possible to uniquely identify each chip using a small digital memory on the chip. However, this identification method is subject to cloning and removal attacks since the digitally stored content can be physically attacked, removed or copied. The signature resulting from the chip's static power tomogram represents the analog leakage variations that cannot be easily controlled, modeled, or cloned [17].

# 4. PRELIMINARIES

This section introduces models for leakage current variation used in the paper and the theory of compressive sensing. We also present the global flow of our approach.

## 4.1 Models for Leakage Current Variation

Process variation is generally categorized as intra-die and inter-die. The inter-die variation represents the variation among different dies in the same wafer. The intra-die variation refers to the variation among different devices on the same chip. Since the inter-die variation in constant over a specific chip, we focus on the inter-die variation.

In the remainder of this paper, we use the model for leakage variation introduced in [10], shown to agree with experimental data. In this model the intra-die variation consists of an uncorrelated random variable and a spatially correlated random variable, both modeled as normally distributed.

Specifically, the Normal random variables describe variation of the gates' dimensions. Because of the exponential relation between the leakage current (static power) and the device dimensions, the leakage current variation distribution is approximately lognormal. Thus, power consumption exhibits multiplicative variation, i.e., $p_u = \phi_u p_u^0$, where $p_u^0$ and $p_u$ are nominal power and real power consumption of the gate $g_u$, respectively, and $\phi_u$ is the scaling factor.

## 4.2 Compressive Sensing

Compressive Sensing is a new signal processing field that exploits sparsity to acquire high-dimensional signals using

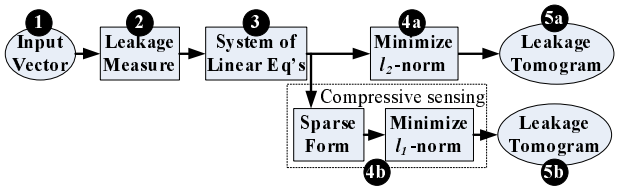


**Figure 1: Global flow of the IC tomography. We can use standard $\ell_2$ norm optimization or compressive sensing to estimate variations.**

very few linear measurements [7,8,18]. Specifically, consider a vector $\mathbf{x}$ in an $N$-dimensional space which is $K$-sparse, i.e., has only $K$ non-zero components. Using compressive sensing, this vector can be sampled and reconstructed with only $M = O(K \log(N/K))$ linear measurements:

$$\mathbf{p} = A\mathbf{x} + e, \tag{1}$$

where $A$ is a $M \times N$ measurement matrix, $\mathbf{p}$ are the measurements and $e$ is the measurement noise.

The sparse vector $\mathbf{x}$ can be recovered from the measurements using the following convex optimization:

$$\min ||\mathbf{x}||_1 + \lambda ||\mathbf{p} - A\mathbf{x}||_2^2, \tag{2}$$

for some appropriate $\lambda$ depending on the noise variance. In the absence of noise, under certain conditions on $A$, (2) exactly recovers $\mathbf{x}$ [8].

This formulation is robust even if the vector is not sparse but is compressible [7,8,18]. A compressible vector has very few significant coefficients and can be well approximated by a $K$-sparse representation. A good model for compressible vectors is the weak $\ell_p$ ball for $p < 1$, i.e., the set of vectors whose coefficients decay as a power law:

$$|\mathbf{x}|_{(i)} \leq r i^{-\frac{1}{p}}, 1 \leq i \leq N \tag{3}$$

where $\mathbf{x} = (x_1, x_2, \ldots x_N)$ and $x_{(i)}$ is $i$-th largest element of $\mathbf{x}$ [8].

In the same framework, a vector might be sparse in a sparsity-inducing basis $W$ instead of the canonical domain. Specifically, if $\mathbf{x} = W\mathbf{s}$, where $\mathbf{s}$ is sparse instead of $\mathbf{x}$, and $W$ is the sparsity-inducing basis, then (1) becomes

$$\mathbf{p} = AW\mathbf{s} + e. \tag{4}$$

Thus the problem is reformulated as the recovery of a sparse $\mathbf{s}$ from $\mathbf{y}$, acquired using the measurement matrix $AW$.

## 4.3 Global Flow

Figure 1 shows the global flow of our method. A number of random input vectors are applied to the circuit, and the leakage current corresponding to each input vector is measured (Steps 1-2). Next, a system of linear equations is formed where each equation corresponds to one measurement (Step 3). The equation unknowns are the (normalized) leakage current variations of each gates. The straightforward way to estimate the IC's leakage tomogram is to use $\ell_2$-norm optimization (Steps 4a-5a). However, our method exploits the sparsity of the statistical leakage variations and the compressive sensing theory to efficiently estimate the leakage tomogram (Steps 4b-5b). Compressive sensing utilizes the $\ell_1$-norm optimization. We compare the quality of the leakage tomograms for $\ell_1$ and $\ell_2$-norm optimizations on standard benchmark circuits.

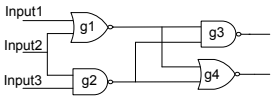


**Figure 2: A simple logic circuit. The power consumption is a function of the input vector.**

| input vector | NAND-2 | NOR-2 |
|---|---|---|
| 00 | 0.776 nW | 17.41 nW |
| 01 | 10.39 nW | 4.112 nW |
| 10 | 4.137 nW | 7.581 nW |
| 11 | 15.15 nW | 3.527 nW |

**Table 1: Static power for different inputs.**

# 5. NONINVASIVE TOMOGRAPHY

This section introduces the complete measurement method for noninvasive gate-level characterization. First, we apply different inputs to the circuit and measure the total chip's leakage current for each input. Then we setup and solve an optimization problem to determine the process variation using the power measurements.

Consider the simple logic circuit in Figure 2 with 3 inputs and 2 outputs. The nominal power consumption of each gate for different inputs is shown in Table I. The table shows the leakage current for 90nm CMOS technology. As a result the circuit has a different power consumptions for each input vector. Because of the process variation, the nominal power consumption of the gate $g_u$ is scaled by $\phi_u$. For example, if inputs 1, 2, and 3 are 0, 1, and 1 respectively, then the power consumption of the circuit, denoted by $p_{011}$, can be expressed as

$$\begin{aligned} p_{011} &= p_{g_1,01}\phi_1 + p_{g_2,11}\phi_2 + p_{g_3,00}\phi_3 + p_{g_4,00}\phi_4 \\ &= 4.112\phi_1 + 15.15\phi_2 + 0.776\phi_3 + 17.41\phi_4, \end{aligned} \tag{5}$$

where $p_{g_i,b_j^i}$ is the consumption of gate $g_i$ for input $b_j^i$. Note that $b_j^i$, the input of each gate $g_i$, is a function of the input vector to the circuit, denoted by $b_j$. For example, in Figure 2, if $b_j = 011$ then $b_j^3 = 00$.

In a digital circuit with $N$ gates, for the binary input vector $b_j$ total power consumption $p_{b_j}$ is

$$p_{b_j} = \sum_{i=1}^{N} p_{g_i,b_j^i}\phi_i. \tag{6}$$

With $M$ input vectors $b_1, ..., b_M$, we define the measurement matrix $A$ as

$$A = \begin{bmatrix} p_{g_1,b_1^1} & p_{g_2,b_1^2} & \cdots & p_{g_N,b_1^N} \\ p_{g_1,b_2^1} & p_{g_2,b_2^2} & \cdots & p_{g_N,b_2^N} \\ \vdots & \vdots & & \vdots \\ p_{g_1,b_M^1} & p_{g_2,b_M^2} & \cdots & p_{g_N,b_M^N} \end{bmatrix}.$$

Also, let $\mathbf{p} = [p_{b_1}, p_{b_2}, \ldots, p_{b_M}]^T, \mathbf{d} = [\phi_1, \phi_2, \ldots, \phi_N]^T$. Then the following system of linear equations determines the gate sizing variations:

$$\mathbf{p} = A\mathbf{d}. \tag{7}$$

With $N$ unknown variables $(\phi_i, i = 1 \ldots N)$ we need $N$ independent measurements to completely determine the solution of (6). However, the measurement vectors are usually dependent. In the presence of power measurement noise, we

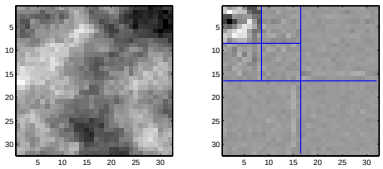

**Figure 3: Process variation and its sparse wavelet transform for a typical circuit. Left variations of a chip in the spatial domain. Right: variations in the wavelet domain.**

can minimize the $\ell_2$-norm of the estimation error:

$$\min ||A\mathbf{d} - \mathbf{p}||_2^2. \tag{8}$$

Each input vector $b_j$ determines a row of the measurement matrix $A$ (power vector), according to the circuit topology. Thus, the rows of the measurement matrix are not necessarily independent. To alleviate this dependency, we use the following input generation method: First, we randomly generate $N_t$ inputs and the corresponding power vectors $\{a_1, a_2 \ldots a_{N_t}\}$. We then select $N_k$ of them as follows: Denote the set of power vectors by $S$ and the subspace of vectors in $S$ by $\mathcal{S}$. Initialize $S = \{a_1\}$. From the remaining power vectors select the $a_i$ with the largest $|a_i^{\perp}|$, where $|a_i^{\perp}|$ is orthogonal component of $a_i$ with respect to $\mathcal{S}$. Add $a_i$ to $S$. Repeat this procedure until $|S| = N_k$.

Even using the above input generation algorithm, it might not be possible to determine the variation of all gates using (8). In the next section, we use compressive sensing to further alleviate this problem.

# 6. FAST TOMOGRAPHY BY COMPRESSIVE SENSING

In this section we model the process variation as a sparse signal, and use compressive sensing to acquire it using very few measurements (fast tomography). We introduce fast tomography for chips with gates on regular grids and then extend this approach for chips with gates on irregular grids.

## 6.1 Sparse Representation

In this section, we use wavelet bases to sparsely model the process variations. Specifically, we assume $\mathbf{d} = W\mathbf{s}$, where $W$ is a wavelet basis and $\mathbf{s}$ is a sparse vector. Wavelet bases are very efficient in sparse modeling of spatial correlation, as shown in the example of Figure 3. The left side of the figure images variations of a chip in the spatial domain, generated using the model in Section 4.1. The right side shows the wavelet transform of the variations. In the wavelet domain most of the non-zero coefficients are concentrated in the upper-left corner of the transform and most of the remaining coefficients are close to zero.

The sparsity induced by various wavelet basis expansions is shown in Figure 4. The figure demonstrates the coefficient decay rate for a variety of wavelet families on typical $32 \times 32$ regular grid circuits generated using the model in Section 4.1. The figure and our preliminary experiments suggest that the Daubechies 9 (db9) wavelet basis is a very good sparsity-inducing basis for the process variation. In the remainder of this paper, we use the Daubechies 9 wavelet to model the sparsity in the process variation.

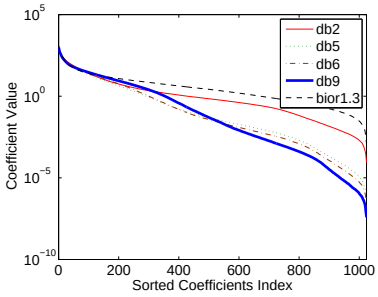


**Figure 4: Sorted wavelet coefficients for different basis functions. The db9 basis produces the sparsest representation.**

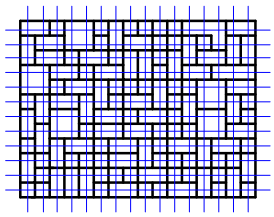

**Figure 5: An example of gates on an irregular grid.**

## 6.2 Regular Grid Tomography

In this section we assume that the logic gates are located on a regular $T \times R$ grid on the chip. The matrxix of process variation on the regular grid is denoted by $H = \{h_{s,t}\}_{s=1\ldots T, t=1\ldots R}$, where $h_{s,t}$ is variation of the gate located at the $(s,t)$-th point of the grid. We stack all the elements of the matrix $H$ in a long column vector $\Phi$.

Using the wavelet basis to model the spatial correlation of the process variation, (7) becomes:

$$\mathbf{p} = A\Phi + e = AW\mathbf{s} + e. \tag{9}$$

The sparse $\mathbf{s}$ can be recovered using (2):

$$\min \|\mathbf{s}\|_1 + \lambda \|AW\mathbf{s} - \mathbf{y}\|_2^2. \tag{10}$$

The process variation $\Phi$ is then recovered using $\Phi = W\mathbf{s}$.

## 6.3 Irregular Grid Tomography

In practice, because of the area and the logic gate constraints, the gates are not located on regular grids. An example of gate placement is shown in Figure 5. We overcome this problem using a dense regular grid such that the center of each gate is close to some grid point for all the gates in the circuit. We assign the variation of each gate $g_u$ to the point on the regular grid that is closest to the center of the gate. If there are more than one closest points, we select one of them randomly. The remaining grid points are assigned to free variables that do not correspond to physical gates and do not affect the measurements.

The remainder of the measurement process is similar to Section 6.2. The points on the regular grid are mapped to a column vector $\Phi$, which is measured by a measurement matrix $A$ as in (9). Note that if the $i$-th element of the $\Phi$ is a free variable not assigned to any gate variation, then $i$-th column of $A$ is zero. The vector $\Phi$ is still spatially correlated and therefore sparse in the wavelet domain, and it can be recovered through $\mathbf{s}$ in (10). In the recovered $\Phi$ the free

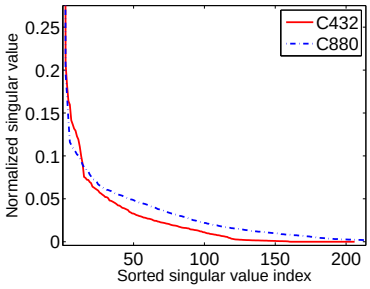


**Figure 6: Sorted singular values.**

variables can be ignored since they do not correspond to physical gates.

# 7. EVALUATION RESULTS

In this section, we evaluate the performance of $\ell_2$-norm optimization and $\ell_1$-norm regularization for chip tomography. After we discuss the power measurement dependency, we compare the $\ell_2$-norm and the $\ell_1$-norm regularization methods on a number of ISCAS'85 benchmarks.

## 7.1 Measurement Matrix Evaluation

The functionality of the IC imposes dependencies in the logic gate statuses. Thus, the power vectors for each input (i.e., the rows of the measurement matrix $A$) are not necessarily independent. In this section we use the Singular Value Decomposition (SVD) to quantify the dependency of the rows of $A$. SVD is a common method for identifying the linear dependency among the vectors.

A matrix with $N$ independent rows has $N$ non-zero singular values. The sorted singular values of C432 and C880 circuits are shown in Figure 6 for a measurement matrix with $M = 6 \times N$ measurements, where $N$ is the number of gates. The singular values for each circuit are normalized such that the largest singular value is 1. The figure shows that the singular values decay rapidly; the 50th singular values in both circuits are less than 5% (0.05).

This decay suggests that it is not possible to find the variation of all gates independently because there is no information about the null space of the measurement matrix, $\mathcal{N}(A) = \{y \in \mathbb{R}^N | Ay = 0\}$. Thus, we can only estimate the variation in a subspace $\mathcal{S}$ that does not contain $\mathcal{N}(A)$.

We use the Gram-Schmidt orthogonalization on the measurement vectors to find a basis for the subspace $\mathcal{S}$. Gram-Schmidt is an efficient sequential procedure that produces an orthonormal basis set from a number of vectors. We use it to efficiently compare the $\ell_2$-norm optimization and the $\ell_1$ regularization methods on the identifiable subspace of the data. We determine that $t$-dimensional subspace using the first $t$ vectors of Gram-Schmidt.

## 7.2 Tomography Results

To study the performance of the proposed tomography method, we simulated the process variation on a number of ISCAS'85 benchmarks using the variation model in Section 4.1. A total of 12% variation is assumed in the simulations. Based on the data in [3] and [12], 20% of the total variation is inter-die variation, 60% is spatial correlated intra-die variation, and 20% is random uncorrelated variation. To model the leakage current (static power), we used the HSpice simulator on 90nm CMOS transistor technology and the DRAGON [19] placement tool.

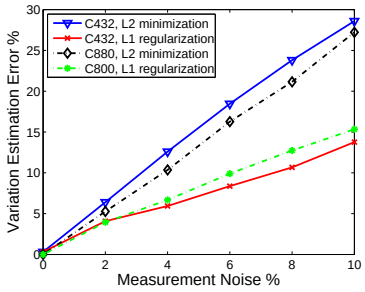


**Figure 7: Variation estimation error vs. percent of the power measurement noise.**

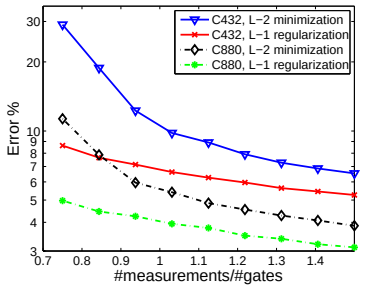


**Figure 8: Variation estimation error vs. number of power measurements.**

Figure 7 presents the variation estimation error for the C432 and the C880 benchmark circuits. The horizontal axis is the power measurement noise and the vertical axis is the variation estimation error. The variation estimation is calculated in a $N/4$-dimensional subspace, where $N$ is the number of gates. Note that by construction the estimation space is orthogonal to the null space of the measurement matrix. Thus, for low noise measurements the $\ell_2$-norm optimization and $\ell_1$-norm regularization are similar. As the noise level increases, the $\ell_1$-norm regularization performs significantly better than the $\ell_2$-norm optimization. For 10% measurement noise, the $\ell_1$-norm regularization estimates the variation about 40% better than $\ell_2$-norm optimization method.

The number of measurements also affects the estimation error. Figure 8 presents the variation estimation error versus number of measurements. The horizontal axis is the ratio of measurements to the total number of the gates in the circuit. The variation is estimated on an $N/4$-dimensional subspace. As the number of measurements increases, $\ell_1$-norm regularization and $\ell_2$-norm optimization have closer performances. It is so because as the number of measurement increases, they cover most of the identifiable directions. Thus sparsity is not as helpful in the reconstruction and the errors of the $\ell_1$-norm and the $\ell_2$-norm optimization become closer.

Table 2 shows tomography results on different benchmark circuits. We used the software package SIS with NAND2, NAND3, NAND4, NOR2, NOR3, NOR4, and inverters to map the circuit to the logic gates. The second column shows the number of gates and the third column reports the number of input pins. For each circuit we used the same number of measurements as the number of gates, reported in the fourth column. The fifth column shows the ratio of the $N/4$-th singular value of the measurement matrix to the 1-st one. The $N/4$ and the $N/7$-dimensional subspaces—the sizes of which are reported in the sixth column—were estimated using the Gram-Schmidt procedure, and both the $\ell_1$ and $\ell_2$-norm optimization methods were evaluated. The

| Circuit properties | | | | | | 3% error | | 6% error | | 9% error | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| name | #gates | #inputs | #meas | $\frac{\sigma_{N/4}}{\sigma_1}$ | subspace | $\ell_1$ error | $\ell_2$ error | $\ell_2$ error | $\ell_2$ error | $\ell_1$ error | $\ell_2$ error |
| C432 | 206 | 36 | 206 | 0.031 | 51 | 4.36 | 5.73 | 7.49 | 11.46 | 10.82 | 17.19 |
| | | | | | 29 | 2.81 | 3.45 | 4.97 | 6.90 | 7.24 | 10.35 |
| C499 | 532 | 41 | 532 | 0.0088 | 133 | 4.45 | 4.67 | 8.15 | 9.04 | 11.97 | 13.48 |
| | | | | | 76 | 2.35 | 2.47 | 4.44 | 4.74 | 6.57 | 7.04 |
| C880 | 353 | 60 | 353 | 0.024 | 88 | 4.66 | 5.62 | 8.76 | 11.24 | 12.94 | 16.86 |
| | | | | | 50 | 3.00 | 3.59 | 5.74 | 7.18 | 8.51 | 10.76 |
| C1355 | 517 | 41 | 517 | 0.012 | 129 | 6.30 | 8.31 | 9.12 | 14.99 | 12.51 | 22.01 |
| | | | | | 73 | 3.58 | 4.37 | 5.35 | 7.84 | 7.37 | 11.48 |
| C1908 | 615 | 33 | 615 | 0.0041 | 153 | 7.06 | 7.46 | 10.93 | 13.71 | 15.24 | 20.19 |
| | | | | | 87 | 2.91 | 3.14 | 4.88 | 5.87 | 7.00 | 8.67 |
| C3540 | 1131 | 50 | 1131 | 0.0067 | 282 | 7.63 | 9.75 | 13.8 | 19.5 | 20.28 | 29.25 |
| | | | | | 161 | 4.68 | 5.50 | 8.63 | 11.79 | 12.72 | 17.69 |
| C5315 | 1796 | 178 | 1796 | 0.007 | 449 | 6.35 | 7.80 | 12.12 | 15.58 | 18.00 | 23.38 |
| | | | | | 256 | 4.04 | 4.72 | 7.82 | 9.40 | 11.63 | 14.10 |
| c8 | 165 | 28 | 165 | 0.040 | 41 | 5.05 | 5.55 | 8.78 | 11.11 | 12.65 | 16.66 |
| | | | | | 23 | 3.21 | 3.43 | 5.45 | 6.86 | 7.80 | 10.29 |

**Table 2: Variation estimation error for different ISCAS'85 benchmark circuits.**

remaining columns demonstrate the results for 3%, 6%, and 9% measurement noise. On average, $\ell_1$-norm optimization performs about 30% better in estimating the variations.

# 8. CONCLUSION

We introduced a new method for noninvasive estimation of the specific leakage variation tomogram for each manufactured chip. The external leakage current measurements were used in a linear optimization framework where the gate leakage variations were the unknowns. Because of the correlations among the gate leakage currents on a chip, the tomogram showing the 2D leakage variations across the IC could be sparsely represented. We exploited the sparsity of the variations in the wavelet domain and the new theory of compressive sensing for fast and efficient estimation of the chip's leakage tomogram. Evaluation results on ISCAS'85 benchmarks demonstrated the effectiveness of the approach. For example, we showed that tomography by compressive sensing in average yields about 30% lower estimation error compared with the traditional least-square estimation.

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