Techniques for Foundry Identification

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ABSTRACT

Foundry identification is essential for many tasks including intellectual property protection, trust, and preventing counterfeiting. In this paper, we introduce statistical techniques for foundry detection, specifically for identifying from which foundry a particular chip originates from. The key idea is to consider the distributions of channel lengths and threshold voltages after employing a variant of SAT that extracts these two metrics. We apply Kolmogorov-Smirnov and other statistical tests for comparing the two empirical distributions. Finally, we study the effects of sample size and measurement error on the correct identification rate and establish an interval of confidence using resubstitution techniques.

1. INTRODUCTION

Integrated circuit (IC) counterfeiting is the unauthorized manufacturing of a chip design without official consent. While this illegal practice reduces the original designer's profits, the extended effects could potentially be much more extreme. Take for example a counterfeit chip made at an untrusted foundry. If such a chip was installed in a life-critical system, such as a medical device or military equipment, the results could be catastrophic.

Since capital costs required to build semiconductor fabrication plants are upwards of one billion US dollars, it is cost prohibitive for chip designers to own and maintain their own private foundries. Instead, they must resort to outsourcing fabrication to third party foundries. Thus, it is imperative that we develop comprehensive techniques for IC trust, intellectual property protection, and counterfeit prevention.

In this paper, we introduce statistical methods for foundry identification. Our techniques enable new applications of foundry identification, including design analysis, yield calculation, and chip usage monitoring.

Our key idea is to use the manifestations of process variation (PV) in integrated circuits, and unique to semiconductor fabrication plants, for the purpose of foundry profiling. Specifically, we use distributions of the following PV-affected parameters, threshold voltage (V_{th}) and effective channel length (L_{eff}). We build foundry profiles consisting of parameter distributions for each design that the foundry is assigned.

While nominal values of V_{th} and L_{eff} are known at design and manufacturing time, due to process variation, they deviate from their expected values [1]. In order to extract the post-silicon physical values, we propose new methods for reverse engineering these parameters. We model simultaneously both the functionality and timing of the integrated circuit. By measuring the delay values made up by a signal edge traversing many gates, we can reverse engineer their individual threshold voltages and effective channel lengths.

Unfortunately, these IC parameters are governed by non-linear models which are difficult to solve for very large systems (e.g. integrated circuits). Thus, we simplify the problem by solving as many linear parts of the system first in order to reduce the complexity and size of the non-linear portions. Specifically, we localize and activate single branches within the IC design using SAT. By measuring the delays of multiple localized branches throughout the circuit we enumerate a system of linear equations for gate delays. Once these linear equations are solved and individual gate delays are known, the non-linear systems that relate delay to V_{th} and L_{eff} are reduced to a single system per gate with as few as two equations, and thus, are much easier to solve.

Once the foundry profiles are characterized, we identify the originating foundry of a particular chip by comparing the parameter distributions of the IC with that of the foundry profile using statistical tests for distribution equality. Furthermore, we investigate and explore the effects of measurement error, sample size, and supply voltage on the identification rate.

2. RELATED WORK

Several foundry identification and IC counterfeiting techniques have been developed. Physical unclonable functions utilize process variation to create unique hardware functions that enable multiple security protocols, including identification [2] [3] [4] [5] [6]. The unique power-up states of SRAM cells have been proposed as IC fingerprints [7]. And passive and active hardware metering schemes enable identification and counterfeit prevention [8] [9].

There exist a number of gate level characterization techniques including direct measurement approaches, methods that incorporate and monitor specialized hardware structures and circuitry, FPGA-based reconfiguration techniques,

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and modeling procedures that assemble systems of equations representing gate characteristics [10] [11] [12]. Applications of gate level characterization include hardware Trojan detection and leakage minimization through post-silicon input vector selection [13] [14] [15].

3. PROCESS VARIATION

Gate delays and effective channel lengths in nanoscale technologies are subject to significant process variation [16] [17]. A variety of manufacturing faults emerge as a result, including but not limited to variations in doping concentrations, imperfect mask alignment, and molecular chemical and physical phenomena. These forms of process variation manifest as the deviation of IC characteristics from nominal values. For example, variations in doping concentrations and line edge roughness alter transistor threshold voltages and effective channel lengths. These manifestations have been thoroughly studied, categorized, and modeled, yet continue to be of paramount concern [18] [19].

4. FOUNDRY CHARACTERIZATION

While the deviation of physical characteristics is inherent within a single chip, the complex and often custom procedures and machinery employed by fabrication facilities make process variations even more pronounced when comparing chips made by different foundries. We build foundry profiles based on these unique parameter deviations.

This enables the identification of an integrated circuit to a particular foundry. We accomplish this by extracting the physical characteristics of the relevant components of a design and comparing its distribution to that of the foundry profile. We investigate the use of transistor threshold voltage and transistor effective channel length distributions of particular designs as the characterizing foundry parameters.

We compare the parameter distributions of an unknown chip of known design with the parameters of a foundry using non-parametric tests for statistical significance in distribution equality, such as the Kolmogorov-Smirnov and Cramér-von Mises tests [20]. These statistical tests are found in common libraries and numerical computing environments, such as the R statistical package and MATLAB. We use the normalized asymptotic p-values (ranging from 0 to 1) to measure similarity strengths. Note, that it is common to reject the null hypothesis, and conclude that two distributions are dissimilar, if the p-value is less than or equal to 0.05.

In the following section we present our methodology for foundry identification in reverse order for clarity. We begin by discussing how to reverse engineer the V_{th} and L_{eff} values of a particular gate using known delay measurements. We then discuss how delay values can be measured for a particular set of gates within the circuit. This discussion also includes how these sets are selected, how to determine the inputs to activate these gates and these gates only, and how to physically measure their total delay.

5. EXTRACTING IC PARAMETERS

We propose a new modeling-based approach to gate level characterization. The model we employ exhibits a non-linear relationship between the IC parameters and delay. Unfortunately, solving this system becomes prohibitively difficult as the system grows in size just beyond a few gates. Since integrated circuits are often composed of orders of magnitude more gates, solving a large set of non-linear equations is entirely impractical.

Therefore, we focus on solving for individual gate delays before solving these non-linear equations. This enables us to separate the system of non-linear equations into individual per-gate systems that can be solved independently. Our first step is to localize these gate delay values. This is accomplished by measuring path delays that consist of some number of gates from an input to an output. This is done by iteratively activating single non-branching paths in the circuit. In this manner, we are able to compose linear equations comprised of the summation of all gate delays along that path (e.g. $D_{path} = d_0 + d_1 + \ldots + d_k$, where D_{path} is the measured path delay and d_i corresponds to the unknown delay of gate i along the path). In order to activate these paths, we systematically search for pairs of inputs using a variant of SAT. We discuss the details of our techniques in the following sections.

5.1 Solving for Threshold Voltage and Effective Channel Length

The threshold voltage and effective channel lengths of each gate can be reverse engineered using Equation 1 from Marković et al. [21]. The two variables subject to the effects of process variation are L_{eff} and V_{th}. In our experiments, we vary the supply voltage (V_{dd}) and measure delay while keeping all other parameters constant.

$$delay = \frac{k_{tp} \cdot k_{fit} \cdot L_{eff}^2}{2 \cdot n \cdot \mu \cdot \phi_t^2} \cdot \frac{V_{dd}}{(ln(e^{\frac{(1+\sigma)V_{dd}-V_{th}}{2 \cdot n \cdot \phi_t}} + 1))^2} \cdot \frac{\gamma_i \cdot W_i + W_{i+1}}{W_i} \quad (1)$$

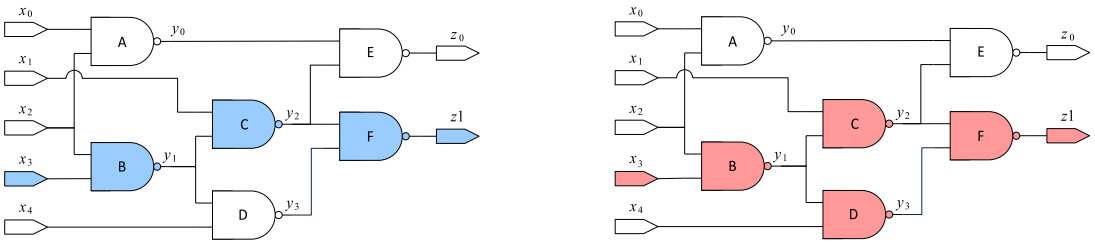
Since this model contains two unknowns, it requires at least two measurements of delay and V_{dd} to create a solvable system of equations. We discuss the details of choosing values of V_{dd} in Section 6.4.

However, physically measuring the delay of a single gate inside of a large circuit is near impossible. Instead, one solution is to solve a system of these equations representing multiple gates whose total delay can more easily be measured. For example, if the critical path is known, then the critical path delay can be measured, which corresponds to the sum of the delays of the gates on the critical path. We discuss the details of activating many different paths for the purposes of building a solvable system of equations in the following section. Unfortunately, due to the non-linearity of this model, solving such large systems is very difficult.

5.2 Solving for Delay

We simplify the large non-linear system described above by reducing it to a set of linear equations comprised of gate delay unknowns (e.g. $D_{path} = d_0 + d_1 + \ldots + d_k$). Once this system of linear equations is solved, each gate's IC parameters can be solved individually and independently using Equation 1. We do this because delay measurements can be localized to single non-branching circuit paths and can be physically measured accurately using clock sweeping techniques.

We build the linear system by selecting sets of gates that each constitute a single non-branching path from input to output and can be activated using appropriate input vectors.



	x_0	x_1	x_2	x_3	x_4	y_0	y_1	y_2	y_3	z_0	z_1
P_0:	1	1	1	0	0	0	1	0	1	1	1
P_1:	1	1	1	1	0	0	0	1	1	1	0
Q_0:	1	1	1	0	1	0	1	0	0	1	1
Q_1:	1	1	1	1	1	0	0	1	1	1	0

Figure 1: Circuit c17 from the ISCAS85 benchmark suite [22]. The blue components in (a) correspond to the signal edge path when initialized with input P_0 followed by applying P_1. The red components in (b) correspond to the signal edge path when initialized with input Q_0 followed by applying Q_1.

These inputs must send the signal edge through these gates and these gates only. Thus, by measuring the delay of the signal edge propagation from input to output, we know the total delay made up of all the individual gate delays along that path.

Take for example Figure 1a. Initializing the circuit with input P_0 followed by applying P_1 causes z_1, y_2, and y_1 to switch. By measuring the delay between sending the signal edge into the circuit (i.e. switching inputs from P_0 to P_1) and measuring the time at which z_1 switches, we can compose a linear equation of the delays of gates B, C, and F that sum to the overall delay. In other words, $D = d_B + d_C + d_F$, where d_i is the delay of gate i.

When applying the Q inputs to the example circuit in Figure 1b, the signal edge follows two paths (colored in red): one through C and the other through D. While this input pair successfully switches output bit z_1, due to race conditions between the C and D gate delays, it is not clear which of the two paths will cause z_1 to switch first. Therefore, the Q input pair cannot reveal any deterministic information about the circuit's individual gate delays.

Note that both the P and Q input pairs are intentionally separated by one hamming distance in order to ensure correct placement of signal edge initiation.

5.2.1 Satisfiability

We employ a variant of SAT in order to find pairs of inputs that satisfy the following constraints:

- Inputs must differ by one hamming distance (i.e. one bit). This ensures accurate placement of signal edge initiation along with precision timing.
- The signal edge must pass through and activate (i.e. switch) only the gates along a single non-branching path. There must be a single and distinct path from the switching input bit to the switching output bit.

We find input vectors that satisfy these constraints by enumerating all paths from input x to output y, then composing the relevant boolean satisfiability constraint and solving.

In Figure 1, only a single path from input x_0 to output z_0 exists and it passes through y_0. Equation 2 defines the constraint for this path. The path from input x_3 to output z_1 is represented by the constraint in Equation 3.

Because this problem is NP-complete and SAT cannot produce an optimal solution, we also conduct an exhaustive search since for a majority of our instances it is possible to enumerate enough solutions to produce a solvable system of equations.

$$f(a) = \begin{cases} True, & \text{if value at wire } a \text{ switches} \\ False, & \text{otherwise.} \end{cases}$$

$$f(z_0) \wedge f(y_0) \\ \wedge f(x_0) \wedge \neg f(x_1) \wedge \neg f(x_2) \wedge \neg f(x_3) \wedge \neg f(x_4) \tag{2}$$

$$f(z_1) \wedge \Big(\Big(f(y_2) \wedge \neg f(y_3)\Big) \vee \Big(\neg f(y_2) \wedge f(y_3)\Big)\Big) \\ \wedge f(y_1) \wedge \neg f(x_0) \wedge \neg f(x_1) \wedge \neg f(x_2) \wedge f(x_3) \\ \wedge \neg f(x_4) \tag{3}$$

5.3 Device Aging

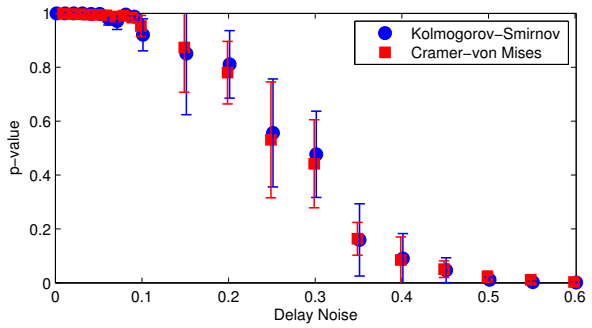
Device aging is a phenomena that changes the physical characteristics (e.g. threshold voltage) of circuit components over time. Even with this added complexity, we can still identify the originating foundry of an aged circuit by employing techniques and models from [23] [24].

By measuring delay and threshold voltage before and after intentional device aging, we enumerate a set of time-dependent non-linear aging model equations as described in Equation 4, then solve for the initial threshold voltage, $V_{th}(t_0)$.

$$V_{th}(t_1) = V_{th}(t_0) + K \times t_1^{0.25} \\ V_{th}(t_i) = V_{th}(t_0) + K \times (t_i - 1 + \Delta T)^{0.25} \tag{4}$$

6. IDENTIFICATION

Correct identification of a circuit largely depends on the precision and accuracy of the delay measurements of each path. In this section we investigate how delay measurement errors, along with path size, supply voltage range, and supply voltage magnitude affect the ability to correctly identify the originating foundry. We also explore the capabilities of our SAT variant in localizing characterizable gates.



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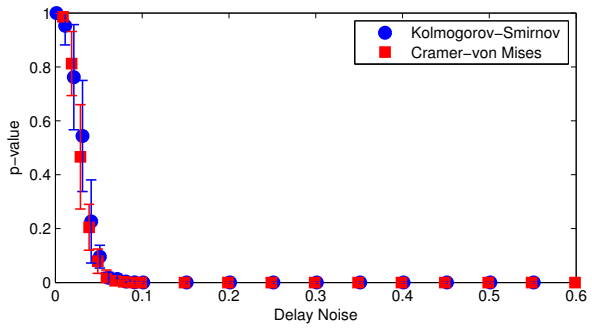
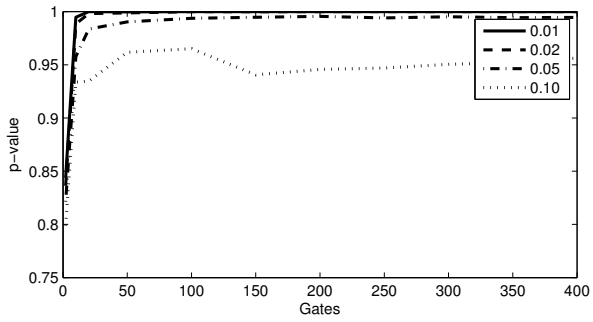


(b)

Figure 2: The effects of delay measurement error on the Kolmogorov-Smirnov and Cramér von-Mises two sample tests for (a) V_{th} and (b) L_{eff}. Uncertainty bars represent the standard deviation of p-values from 100 tests.



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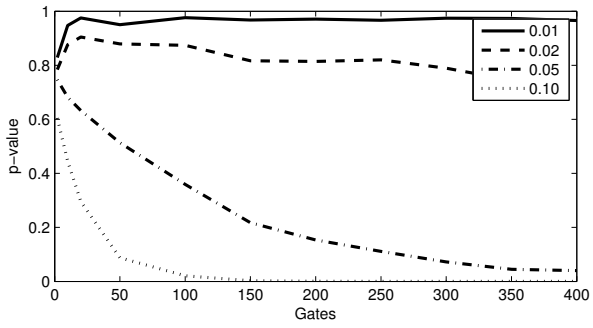


(b)

Figure 3: The effects of distribution size and delay measurement errors on correct identification using distributions of (a) V_{th} and (b) L_{eff}. Legend errors correspond to those described in Figure 2.

6.1 Delay Measurement Error

We investigate the resilience of our techniques to natural fluctuations and error in delay measurement. We introduce a gaussian error whose standard deviation is multiplied by the expected delay and the fraction depicted on the x-axis in Figure 2. The figure comprises of p-values comparing the foundry profile parameters to the reverse engineered IC parameters of a branch of 200 gates with a range of supply voltages from 0.5V to 3V. The remaining figures in this paper depict p-values generated using the Kolmogorov-Smirnov test.

Correct characterization through reverse engineering of V_{th} is resilient up to an error rate of 0.4, while the characterization of L_{eff} tapers and fails the test at about 0.05. Depending on the apparatus and techniques available to us as well as the level of certainty required, either one or both of these characteristics can be utilized for identification.

6.2 Sample Size

The asymptotic p-value for the Kolmogorov-Smirnov two sample test becomes very accurate for large sample sizes. It is also assumed to be reasonably accurate for sample sizes n_0 and n_1 such that $\frac{n_0 n_1}{n_0+n_1} \geq 4$. However, the measurement error in delay—which consequently translates to error in the reverse engineered values of V_{th} and L_{eff}—has a complex effect on the ability of the statistical test to measure distribution equality.

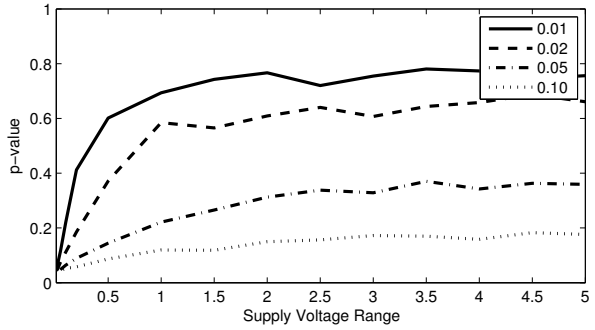
Figure 3 shows that even with a substantial amount of delay measurement error, a circuit can be correctly identified using V_{th} parameters, while for L_{eff} the increasing error rate has a negative effect on the ability of the statistical test to correctly identify the foundry. So long as measurement error is low, we can use both characteristics to model and identify foundries. For higher error rates, V_{th} should be used.

Table 1: Gates in benchmark circuits [25] [26] whose IC parameters can be fully characterized.

Circuit	Total Gates	Characterized Gates
s9234	5,597	1,165
s15850	9,772	3,994
b21_1	12,248	138
b20_1	12,264	138
s35932	16,065	4,754
b20	17,158	138
b21	17,482	138
b22_1	18,461	170
s38584	19,253	4,878
s38417	22,179	6,274
b22	25,460	154
b17	27,852	759
b17_1	32,971	860
b18_1	88,954	590
b18	94,249	582

6.3 Gate Delay Characterization

We evaluate our techniques using the ISCAS89 and ITC99 benchmark suites [25] [26]. Table 1 lists the total number of gates we are able to characterize using our SAT formulation. Specifically, the equations extracted comprise a solvable system for the individual gate delays of each benchmark circuit. We employ a linear solver to calculate the gate delays across a span of supply voltage magnitudes and ranges.



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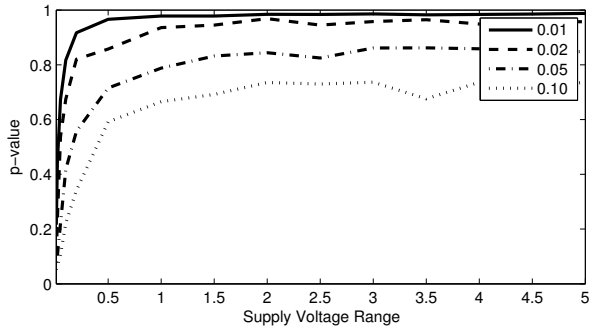
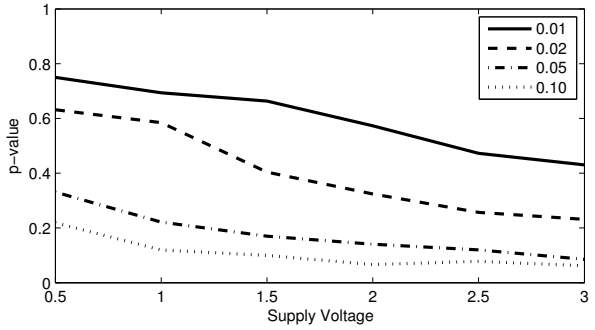


(b)

Figure 4: The effects of supply voltage range on correct identification using distributions of (a) V_{th} and (b) L_{eff}. The first voltage equals 1V while the second voltage differs by the value along the x-axis. Legend errors correspond to those described in Figure 2.



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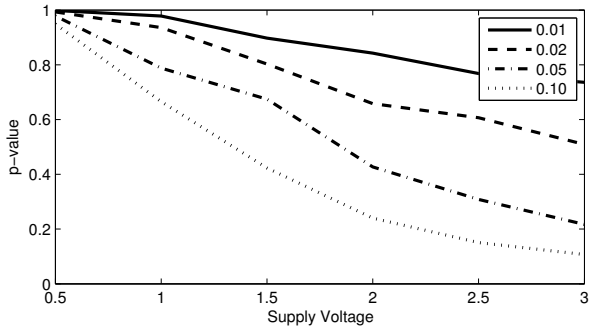

(b)

Figure 5: The effects of supply voltage magnitude on correct identification using distributions of (a) V_{th} and (b) L_{eff}. The first supply voltage corresponds to the value along the x-axis. The second supply voltage is 1V larger. Legend errors correspond to those described in Figure 2.

6.4 Supply Voltage Range and Magnitude

We find that the number of supply voltages required to create a solvable system for reverse engineering V_{th} and L_{eff} using Equation 1 has a very limited impact on the correct identification rate as compared to the *selection* of supply voltages. Thus, we construct our system using the minimal required number of equations and investigate the selection—focusing on magnitude and range—of supply voltages.

Our first observation found in Figure 4 confirms that increasing the distance between the two supply voltages governing the system of equations improves the overall identification rate of a circuit. Our second observation found in Figure 5 confirms that the magnitude of the supply voltage pair (given a predetermined range) is best applied nearer to the nominal threshold voltage rather than far away. The first observation is explained given the resulting collinear results of the non-linear model (Equation 1) when two supply voltages are placed close to one another. Likewise, the delay model becomes collinear at large supply voltages, while at near-threshold values, the non-linear relationship between supply voltage and delay is much more pronounced and can be solved much more accurately.

6.5 Foundry Identification

We test the overall resilience of our techniques by identifying the originating foundry of many instances of three chips in a simulated environment with a 0.05 delay measurement error rate. Simulation parameters are depicted in Figure 6. The foundries A, B, and C are represented by their IC parameter distributions as governed by their unique process variations. Circuits 1, 2, and 3 are example instances corresponding to foundries A, B, and an unknown site, respectively. After reverse engineering the IC parameters of circuits 1, 2, and 3 we overlay the resulting predicted IC parameters in Figure 6.

The Kolmogorov-Smirnov two sample test results comparing the threshold voltage and channel length distributions between each pair of circuit and foundry are listed in Table 2. The threshold voltage comparisons successfully identify foundries A and B as the originating fabrication facilities of circuits 1 and 2, respectively, as well as rejecting circuit 3 from all three foundries. However, the effective channel length distribution tests for both circuit 1 and 2 are not as reliable as they periodically dip below an acceptable significance level of 0.05.

7. CONCLUSION

We have presented new statistical techniques for foundry detection by specifically identifying from which foundry a particular chip originates from. Our key idea is to consider the distributions of channel lengths and threshold voltages by assembling and solving a variant of SAT, then focus on solving the linear parts of the system as far as possible before reverse engineering the IC parameters. We then compared the IC parameter distributions using non-parametric statistical tests in order to identify the originating foundry.

We have tested our techniques on a host of benchmark circuits while investigating the effects of delay measurement error, sample size, and voltage range and magnitude on the

correct identification rate. We find that reverse engineered threshold voltage distributions are resilient to high delay measurement error while effective channel lengths are resilient only at very low error rates.

8. ACKNOWLEDGEMENTS

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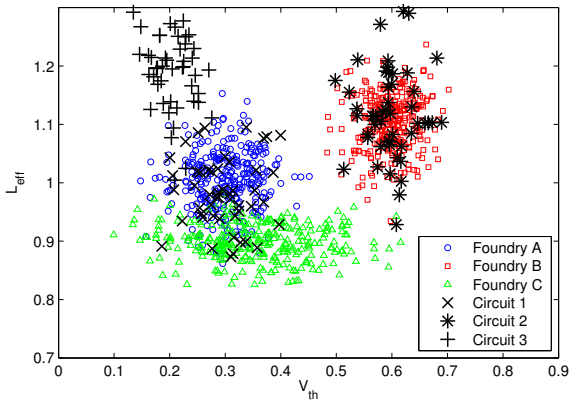

Figure 6: IC parameters and foundry profiles. Circuit 1 originates from foundry A, circuit 2 originates from foundry B, and circuit 3 is a counterfeit that does not originate from any trusted foundry. The circuit parameters are reverse engineered from delay values measured with a 0.05 error rate.

Table 2: Minimum and maximum p-values for circuit parameter and foundry profile comparisons using the Kolmogorov-Smirnov test. Foundry distributions correspond to those depicted in Figure 6. We test 20 instances of each circuit.

		Foundry A	Foundry B	Foundry C
Circuit 1	V_{th}	0.35 - 0.96	0	0
	L_{eff}	0 - 0.80	0	0
Circuit 2	V_{th}	0	0.24 - 0.76	0
	L_{eff}	0	0.02 - 0.69	0
Circuit 3	V_{th}	0	0	0
	L_{eff}	0	0	0

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